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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,767	10/12/2005	**Jeroen Anton John Leijten**	260692	2219

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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/552,767	LEIJTEN, JEROEN ANTON JOHN	
	Examiner	Art Unit	
	DAVID J. HUISMAN	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6-8,12 and 13* is/are rejected.

7)☒ Claim(s) *2,3,5 and 9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3 and 5-13 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Extension of Time as received on 4/16/2009.

Claim Objections

3. Claims 1-3 and 5-8 are objected to because of the following informalities:

- It is asked that applicant use other language that "characterized in that". It is not clear what entities, in claims 1 and 8, for instance, are "characterized in that…". The word "wherein" is more commonly used and would be a better alternative.

4. Claims 2-3 and 5-7 are objected to because of the following minor informalities: In line 1 of each of the claims, replace "A processor" with --The processor--.

5. Claim 8 is objected to because it is not clear if applicant is attempting to claim a processor or a method. Please ensure that only method steps are claimed if applicant wants to claim a method. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 2-3, 5, and 9-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, claims 2 and 9 set forth that the operation is a NOP operation and that the writing of result data corresponding to the operation into the register file is dynamically controlled. The examiner is not aware of a NOP that actually produces result data, as a NOP an instruction that does nothing. Applicant has not enabled a NOP that produces a result. Therefore, applicant must either clarify the claims or point to support in the specification which sets forth how to make and use a NOP which produces a result.

8. Claims 3, 5, and 10-11 are rejected under 35 U.S.C. 112, 1st paragraph, for lacking enablement, because they are each dependent on a claim that is not enabled.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 6, 8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp et al., U.S. Patent No. 5,748,936 (herein referred to as Karp), in view of Kogge, "The Microprogramming of Pipelined Processors," 1981 (herein referred to as Kogge).

11. Referring to claim 1, Karp has taught a processor arranged for execution of a program, the processor comprising:

a) a plurality of execution units, comprising at least a first execution unit and a second execution unit. See Fig,2, components 30.

b) a register file accessible by the execution units. See Fig.2, components 32, and column 5, lines 7-8. Note that one register file may exist, or multiple register files may exist, where in the case of multiple register files, each would be a sub-file making up an overall register file.

c) a communication network for coupling the execution units and the register file. See Fig.2. Clearly, execution units must be coupled to the register file(s).

d) a controller arranged for controlling the processor based on control information derived from the program, characterized in that at least the first execution unit and the second execution unit are each arranged to produce, according to a programmed criterion specified within said program, a second identifier on validity of an output result for corresponding output ports of the first and second execution units, the processor being arranged to dynamically control writing of result data corresponding to an operation into the register file, based at least on the second identifier and without performing a jump operation. See Fig.5 and column 10, lines 1-60. Note that result writing is based on predicate, poison bit, and exception information. At least one of these items qualifies as the second identifier. For instance, the second identifier may be considered the poison bit, which is set based on whether an exception was generated (result invalid) or not generated (result valid). It should be further noted that the setting of the bit is performed according to a programmed criterion. That is, everything a processor does is according to some programmed criterion set forth by the program. In this case, the processor is

programmed to write a particular value in a poison bit according to detection of an exception/error. For example, the processor is able to detect that a floating-point exception occurs, and that a poison bit should be set in response to such an exception, because the system has been programmed to look for floating-point errors (column 10, lines 43-45). Note that no jumps occur in the process of Fig.5. All of the exceptions detected are deferred, so the register file writing is controlled with performing a jump.

e) Karp has taught a data-stationary processor but has not taught a time-stationary processor, as known in the art. However, Kogge has taught the concepts of both data-stationary and time-stationary control. More importantly, Kogge has taught that a pipeline can support both types of controls. See the 1st full paragraph on page 65. The implementation of time-stationary control requires the hardware of Fig.2(a) and the implementation of data-stationary control requires the hardware of Fig.2(b). Hence, it can be seen that implementing time-stationary control requires fewer buffers (less hardware) than its counterpart. Consequently, it would have been obvious to one of ordinary skill in the art to modify Karp to include time-stationary control as opposed to data-stationary control. One would be motivated to make such a combination to reduce hardware cost, and further, the producing an identifier on validity of a result would still apply because time-stationary processors are able to support conditional branches. See page 67, column 2, and page 68. The validity identifier in Karp is produced in response to branch instructions when speculative execution begins.

12. Referring to claim 6, Karp in view of Kogge has taught the processor according to claim 1, characterized in that the register file is a distributed register file. See Fig.2 and note that a

register file is divided into multiple sub-register files 32) which are distributed throughout the system for use by the execution units.

13. Referring to claims 8 and 12, claims 8 and 12 are rejected for the same reasons set forth in the rejections of claims 1 and 6 above, respectively.

14. Claims 2-3, 5, and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp in view of Kogge and further in view of Jen et al., U.S. Patent No. 5,031,096 (herein referred to as Jen).

15. Referring to claim 2, Karp in view of Kogge has taught a processor according to claim 1. Karp, as modified, has not taught that the control information further comprises a first identifier on the validity of the operation, the first identifier indicating that the operation is invalid in a case where the operation is a NOP operation, and wherein the processor is arranged to dynamically control writing of result data corresponding to the operation into the register file, based on both the first identifier and the second identifier. However, Jen has taught including an invalid bit when an instruction is detected to be a NOP. See claim 1 of Jen, for instance. This invalid bit allows Jen to compress execution by replacing an invalid operation with a valid operation. See column 2, lines 11-44. Such a bit controls writing of data because if an invalid operation executes, no data will be written. If a valid operation executes, data will be written. So, if a valid operation executes in the invalid operation's place, then data will be written to the register file sooner. Therefore, in order to compress execution, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Karp such that the control information further comprises a first identifier on the validity of the operation, the first identifier

indicating that the operation is invalid in a case where the operation is a NOP operation, and wherein the processor is arranged to dynamically control writing of result data corresponding to the operation into the register file, based on both the first identifier and the second identifier.

16. Referring to claim 3, Karp, as modified, has taught a processor according to claim 2, characterized in that the first identifier is delayed according to the pipeline of the corresponding execution unit arranged for executing the operation. See claim 1 of Jen, and Fig.5. Essentially, after the instruction is tagged with its valid bit, it is first moved to an adjacent register before it is executed. Hence, the first identifier is delayed by at least the time required to move it from a first register to a second register.

17. Referring to claim 5, Karp, as modified, has taught a processor according to claim 3, characterized in that the processor is further arranged to dynamically control writing of result data corresponding to the operation into the register file, based on the first identifier, the second identifier and an input datum. See Karp, Fig.5, and note that each of the first identifier (valid/invalid), the second identifier (exception), and an input datum (either poison bit shown in Karp, Fig.5, step 208, the predicate information set forth in Karp, Fig.5 and column 10, lines 1-21 (Essentially, at any point before results are to be written, if it is determined that a predicate is false and that an instruction should not modify the state of the system, result data is not written to the register file. If the predicate is true, then result data could be written to the register file if other factors are satisfied), or the result itself, which is an input to the register file) plays a role in controlling writing to the register file.

18. Referring to claims 9-11, claims 9-11 are rejected for the same reasons set forth in the rejections of claims 2-3 and 5 above, respectively.

19. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Karp in view of Kogge and further in view of the examiner's taking of Official Notice.

20. Referring to claim 7, Karp in view of Kogge has taught the processor according to claim 1. Karp has not explicitly taught that the communication network is a partially connected communication network. However, Official Notice is taken that partially connected communication networks, and their advantages, are well known and accepted in the art. A partial network is where at least one execution unit is coupled to less than N register files. One example would be where integer circuitry is couple to an integer register file and floating-point circuitry is connected to a floating-point register file. Since, integer circuitry does not operate of floating-point numbers or write floating-point numbers, then the integer unit does not have to be coupled to the floating-point register file. Clearly, by requiring less wiring than a fully connected network, the partial network is less expensive in terms of silicon. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Karp such that the communication network is a partially connected communication network.

21. Referring to claim 13, claim 13 is rejected for the same reasons set forth in the rejection of claim 7 above.

Response to Arguments

22. Applicant's arguments filed on April 16, 2009, have been fully considered but they are not persuasive.

23. Applicant argues the novelty/rejection of claim 1 on pages 5-7 of the remarks, in substance that:

> "Claims 1 and 8 have been amended, in accordance with the examples of programmed operation sequences provided on page 8, line 22 to page 12, line 27, to recite that dynamically controlling the writing of result data into the register file is carried out without performing a jump operation. Karp, in contrast to the claimed invention, relies upon branching (conditional jumping) to an exception handling routine to dynamically control writing of result data into the register file."

24. These arguments are not found persuasive for the following reasons:

a) When looking at Fig.5 and column 10, lines 1-60, one would realize that Fig.5 is a process for deferring exceptions and controlling register file writes during speculative execution of instructions. Hence, in step 212, even if an exception is generated, a jump to an exception handler does not occur at this point. Instead, the poison bit is set and the exception is deferred until some safe point. Hence, the controlling of result-writing to the register file occurs without performing a jump operation. If an exception is not generated in step 212, then the processor allows the result to be written. This alone controls the writing without performing a jump. And, as stated above, if an exception is generated in step 212, then the processor prevents the result from being written. This prevention is also accomplished without performing a jump because a jump is not performed at this point (since the exception handling is deferred).

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Terada et al., U.S. Patent No. 6,041,399, has taught a VLIW system with predicated instruction execution for individual instruction fields.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. HUISMAN whose telephone number is (571)272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183
May 21, 2009